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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/084,569	02/27/2002	Ahmad R. Ansari	X-987 US	7959

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XILINX, INC
ATTN: LEGAL DEPARTMENT
2100 LOGIC DR
SAN JOSE, CA 95124

EXAMINER	
CERULLO, JEREMY S	

ART UNIT	PAPER NUMBER
2112	

DATE MAILED: 10/01/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/084,569	ANSARI ET AL.	
	Examiner	Art Unit	
	Jeremy S. Cerullo	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 February 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-34* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 February 2002* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☒ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *20020429, 20040120*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

1. The information disclosure statement filed January 20, 2004, fails to comply with 37 CFR 1.98(a)(2), which requires a legible copy of each U.S. and foreign patent; each publication or that portion which caused it to be listed; and all other information or that portion which caused it to be listed. It has been placed in the application file, but the information referred to therein has not been considered.

The examiner has considered and initialed those documents present in the application file on the IDS forms accompanying the instant office action. Foreign patent and non-patent documents not present in the application file have been lined out on the form. Applicant should resubmit the missing documents to ensure proper consideration.

Oath/Declaration

2. The oath or declaration is defective. A new oath or declaration in compliance with 37 CFR 1.67(a) identifying this application by application number and filing date is required. See MPEP §§ 602.01 and 602.02.

> The oath or declaration is defective because:
> It does not identify the mailing address of each inventor. A mailing address is an address at which an inventor customarily receives his or her mail and may be either a home or business address. The mailing address should include the ZIP Code designation. The mailing address may be provided in an application data sheet or a supplemental oath or declaration. See 37 CFR 1.63(c) and 37 CFR 1.76.
>
> It does not identify the city and either state or foreign country of residence of each inventor. The residence information may be provided on either on an application data sheet or supplemental oath or declaration.

Drawings

3. The drawings are objected to because of inconsistencies between Figure 1 and its detailed description in the specification. The sample cycle signal 128 should be shown going from the slave sample cycle generator 118 to the slave 108, and the slave's internal clock signal 132 should be shown going from the slave 108 to the slave sample cycle generator 118.

4. The drawings are objected to because a dashed signal line in figure 6, between Master 1 and the Bus Arbiter is not appropriately labeled.

5. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description: 800.

6. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference character(s) not mentioned in the description: 828 and 836.

7. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate

changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

8. The disclosure is objected to because of the following informalities: In the third line of paragraph [0062], the bus arbiter is referenced with label 636, whereas in the figure, the bus arbiter is labeled 628.

In lines 8-11 of paragraph [0063], it is stated that state machines 648, 652, and 656 are within slaves 616, 608, and 612, respectively. According to figure 6, state machines 648, 652, and 656 are within slaves 608, 612, and 616, respectively.

Appropriate correction is required.

9. The specification is objected to as failing to comply with 37 CFR 1.74 because the following reference character(s) are not mentioned in the description: 828 and 836.

10. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 102

11. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

12. Claims 5-6 and 19 are rejected under 35 U.S.C. 102(b) as being anticipated by Billings et al. (U.S. Patent No. 5,867,694).

A. As for Claim 5, Billings discloses a method for generating sample cycle pulses (Figure 4; Column 3, Line 44 – Column 4, Line 11), determining a ratio of an internal clock to the clock of a bus (Column 1, Line 61 – Column 2, Line 8), and generating a sample cycle pulse in an appropriate cycle (Figure 4; Column 3, Line 44 – Column 4, Line 11).

B. As for Claim 6, Billings discloses the use of clock speed ratios in the form of N:2 (Column 1, Line 61 – Column 2, Line 8). This is equivalent to determining a ratio of clocks by counting the clock pulses of the faster clock in two pulses of the slower clock, and dividing by two.

C. As for Claim 19, Billings discloses a device comprising at least one input port, circuitry for determining a frequency, circuitry for determining a ratio between two clocks, and circuitry for determining when to latch communication signals. See Figure 6 and Column 1, Line 61 – Column 2, Line 8 and Column 5, Lines 29-43.

13. Claims 10-12, 14-15, and 17 are rejected under 35 U.S.C. 102(b) as being anticipated by Kelley et al. (U.S. Patent No. 6,134,621).

A. As for Claim 10, Kelley discloses a method for selecting a bus frequency comprising: setting a bus frequency according to the identity of the devices that will be a part of the transaction (Figures 3-5 and Column 1, Lines 31-49), and setting a bus frequency so that any receiver of for the communications of the transaction will have a frequency that is an integer multiple of the bus frequency (Figures 3-5 and Column 1, Lines 31-49). In U.S. Patent No. 6,134,621, the possible bus and device speeds are 33 MHz and 66 MHZ. The bus will only run at 66 MHz if there are only 66 MHz devices. Therefore the device speeds are integer (1) multiples of the bus speed. If there are any 33 MHz devices, the bus operates at 33 MHz. Therefore, the device speeds are also integer (1 for 33 MHz devices, and 2 for 66 MHz devices) multiples of the bus speed.

B. As for Claim 11, Kelley discloses determining the internal frequency of the bus (Column 1, Lines 31-49).

C. As for Claim 12, Kelley discloses determining the internal frequency of a slave or receiver device (Column 1, Lines 31-49).

D. As for Claim 14, Kelley discloses determining bus frequency dynamically (Column 1, Lines 31-49).

E. As for Claim 15, Kelley discloses that bus frequency is determined according to the length of the bus and the amount of devices on the bus (Column 1, Lines 11-49). This is done to limit the impedance on the line caused by distance between devices and any additional devices on the circuit.

F. As for Claim 17, Kelley discloses that the frequency of the bus is determined by a clock generation controller (Figure 1, Element 111).

14. Claims 30-34 are rejected under 35 U.S.C. 102(b) as being anticipated by Solomon (U.S. Patent No. 5.943,483).

A. As for Claim 30, Solomon discloses a system comprising: a port; a bus; a bus master coupled between the port and the bus; a processor coupled to the bus; and a memory device coupled to the bus, wherein the memory device comprises a memory portion storing data that defines arbitration logic for the bus. See Figure 3 and Column 4, Lines 1-40.

B. As for Claim 31, Solomon discloses that the data comprises computer instructions for the processor (Column 4, Lines 17-40).

C. As for Claim 32, Solomon discloses the memory device stores computer instructions for the processor that define ordinary operation of the system (Column 4, Lines 12-40).

D. As for Claim 33, Solomon discloses that the system comprises an ASIC (Column 4, Lines 1-11).

E. As for Claim 33, Solomon discloses that the system comprises dedicated hardware logic (Column 4, Lines 1-11).

Claim Rejections - 35 USC § 103

15. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

16. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

17. Claims 1-4, 16, and 21-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Solomon (U.S. Patent No. 5,943,483) and Kelley et al. (U.S. Patent No. 6,134,621).

A. As for Claim 1, Solomon teaches a system comprising: first and second bus masters; first and second slaves; a bus coupled to the first and second bus masters and the first and second slaves; and a bus arbiter comprising at least one port (Figure 2). However, Solomon does not teach logic circuitry that

defines logic to select a bus frequency for the requested transaction. Kelley teaches logic circuitry (Figure 1, Element 121; Column 2, Line 1 – Column 3, Line 54) that defines logic (Figure 3) to select a bus frequency. It would have been obvious to one of ordinary skill in the art at the time of the invention to use the logic circuitry of Kelley in the arbiter of Solomon. One would have been motivated to do so in order to allow for the use of one or two higher speed devices (66MHz) on the bus, while allowing the system to slow down to accommodate slower devices or more devices (Kelley - Column 1, Lines 30-50).

B. As for Claim 2, Kelley's teaching that the bus frequency depends on the capabilities of the devices (33 MHz or 66MHz) (Column 1, Lines 30-50) is equivalent to the instant application's limitation of the logic circuitry defining the logic to select a bus frequency according to the identity of the slave.

C. As for Claim 3, Kelley's teaching that the bus frequency depends on the capabilities of the devices (33 MHz or 66MHz) (Column 1, Lines 30-50) is equivalent to the instant application's limitation of the logic circuitry defining the logic to select a bus frequency according to the identity of the master.

D. As for Claim 4, Kelley's teaching that the bus frequency depends on the number of devices (or segments) on the PCI bus (Column 1, Lines 30-50) is equivalent to the instant application's limitation of the logic circuitry defining the logic to select a bus frequency according to the length of the bus.

E. Claim 16 is rejected as being unpatentable over Kelley, as applied to Claim 10, and its combination with Solomon, as applied to Claim 1. In the rejection of Claim 1, the examiner gave the motivation for including the logic circuitry of Kelley in the arbiter of Solomon.

F. Claims 21-24 contain the same limitations as Claims 1-4, respectively, and are therefore rejected on the same basis as Claims 1-4.

G. As for Claim 25, Solomon also teaches that the arbiter can be processor based. See Figure 3.

H. As for Claim 26, Solomon also teaches that the arbiter can comprise an application-specific integrated circuit. See Column 4, lines 1-11.

18. Claim 7 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Billings et al. (U.S. Patent No. 5,867,694) as applied to claims 5-6 above, and further in view of Summer, Jr. et al. (U.S. Patent No. 4,414,624).

A. As for Claim 7, Billings teaches determining bus frequency, comparing the internal clock frequency to the frequency of the bus, generating sample cycle signals, and latching data onto the bus (See Figure 4 and Column 1, Line 61 – Column 2, Line 8). However, Billings does not teach generating a request for access or control of the bus, receiving a grant from a bus arbiter, or the issuing of a release signal upon termination of the transaction. Summer, Jr., does teach these limitations. In Figure 3, Summer, Jr., teaches arbitration scheme that includes a bus request, a grant assertion to said request, and clear grant signal that releases the bus. These steps are equivalent to the limitations in

Claim 7 of the instant application that are not taught by Billings et al. One of ordinary skill in the art at the time of the invention would have been motivated to combine the arbitration method of Summer, Jr., with the timing method of Billings in order to allow for a synchronized arbitration method capable of utilizing multiple devices (Summer: Column 1, Lines 26-41).

B. As for Claim 9, Billings et al. also teaches that the sample signal is used to indicate when data is to be latched and that data can be written after the sample signal goes low. See Figure 4 of reference.

19. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Billings et al. and Summer, Jr., et al. as applied to claim 7 above, and further in view of Butler, Jr., et al. (U.S. Patent No. 3,708,686). Billings and Summer do not teach the additional limitation of determining the relative difference between the internal clock frequency and the bus clock frequency by counting the falling edges of the clock cycles for the internal clock in two periods of the bus clock. However, Butler does teach that a count of the number of initiations of a clock signal within any fixed time interval provides a measure of the difference between the frequencies of the two clocks (Column 18, Lines 9-15). It would have been obvious to one of ordinary skill in the art at the time of the invention to use the method of comparing clocks according to Butler, Jr., within the communication method taught by Billings and Summer, Jr. One would have been motivated to use the fixed time period in order to have a consistent measurement of the clock frequencies for comparison (Summer: Column 17, Line 50 – Column 18, Line 15).

20. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kelley et al. as applied to claim 10 above, and further in view of Lee et al. (U.S. Patent No. 6,611,893). Kelley teaches the step of determining the identity of the devices in a transaction, but Kelley does not teach the step of examining a table to determine frequency. Lee teaches the use of a look up table to determine the speed of source and destination devices (Column 3, Lines 49-58). It would have been obvious to one of ordinary skill in the art at the time of the invention to use a look-up table as taught by Lee in the system taught by Kelley. One's motivation for doing so would have been to eliminate the delay that would have been caused by forcing the system to determine the speeds of devices dynamically (Lee: Column 3, Lines 49-58).

21. Claim 18 rejected under 35 U.S.C. 103(a) as being unpatentable over Kelley et al. and Solomon as applied to claim 16 above, and further in view of Eikill et al. (U.S. Patent No. 5,131,085). Kelley and Solomon teach the method wherein a bus arbiter determines the bus frequency. They do not teach a method wherein a bus master determines the bus frequency. However, Eikill teaches that bus arbitration can be performed by individual bus masters (Column 3, Lines 10-25). One of ordinary skill in the art at the time of the invention would have been motivated to include the arbitration of Kelley and Solomon in the bus masters of Kelley and Solomon according to the method taught by Eikill in order to more effectively employ a shared bus (Eikill: Column 3, Lines 10-25).

22. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Billings et al. as applied to claim 19 above, and further in view of Ogletree (U.S. Patent No. 5,579,477). Billings teaches a sample cycle signal used to prompt the slave to latch the communication signals (Figure 4). However, Billings does not teach the use of a state machine to generate the sample cycle signal for prompting the slave to latch the communication signals. Ogletree teaches the use of a state machine to generate a clock signal (Column 7, Lines 10-33). The clock signal generated by the state machine is equivalent to the sample cycle signal claimed in the instant application. It would have been obvious to one of ordinary skill in the art at the time of the invention to use a state machine as taught by Ogletree to generate the latching sample signal of Billings. One would have been motivated to do so in order to have a sample signal that could adjust with a changing clock frequency (Ogletree: Column 7, Lines 10-33).

23. Claim 27 is rejected under 35 U.S.C. 103(a) as being unpatentable over Solomon and Kelley et al. as applied to claim 26 above, and further in view of Ghori (U.S. Patent No. 6,243,772). Solomon and Kelley teach the inclusion of hardware logic that performs arbitration tasks (Column 4, lines 1-11 of Solomon; See rejection of Claim 26 above), but they do not teach that said dedicated hardware logic (ASIC in Solomon) performs table lookup tasks. Ghori teaches that an ASIC can use look-up tables stored in memory to assist in performing its tasks (Column 10, Lines 40-50). It would have been obvious to one of ordinary skill in the art at the time of the invention to use an ASIC

capable of using look-up tables as taught by Ghori in the arbiter as taught by Solomon and Kelley et al. The motivation for doing so would be advantageous to have arbitration functions stored in a look-up table in order to increase the speed and efficiency of the arbitration (Lee: Column 3, Lines 49-58).

24. Claim 28 is rejected under 35 U.S.C. 103(a) as being unpatentable over Solomon and Kelley et al. as applied to claim 21 above, and further in view of Billings et al. as applied to claim 19 above. Solomon and Kelley do not teach the specifics of the slave claimed in the dependent claim 28. However, Billings does teach system that has at least one input port, circuitry for determining a frequency, circuitry for determining a ratio between clocks, and circuitry for determining when to latch communication signals. See Figure 6 and Column 1, Line 61 – Column 2, Line 8 and Column 5, Lines 29-43. It would have been obvious to one of ordinary skill in the art at the time of the invention to use the device taught by Billings as the slave in the system of Solomon and Kelley. One would have been motivated to do so in order to allow the slave to communicate at varying frequencies (Ogletree: Column 7, Lines 10-33).

25. Claim 29 is rejected under 35 U.S.C. 103(a) as being unpatentable over Solomon, Kelley et al., and Billings et al. as applied to claim 28 above, and further in view of Ogletree as applied to claim 20 above. Billings teaches a sample cycle signal used to prompt the slave to latch the communication signals (Figure 4). However, Billings does not teach the use of a state machine to generate the sample cycle signal

for prompting the slave to latch the communication signals. Ogletree teaches the use of a state machine to generate a clock signal (Column 7, Lines 10-33). The clock signal generated by the state machine is equivalent to the sample cycle signal claimed in the instant application. It would have been obvious to one of ordinary skill in the art at the time of the invention to use a state machine as taught by Ogletree to generate the latching sample signal of Billings. One would have been motivated to do so in order to have a sample signal that could adjust with a changing clock frequency (Ogletree: Column 7, Lines 10-33).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeremy S. Cerullo whose telephone number is (703) 305-6435. The examiner can normally be reached on Monday - Thursday, 6:45-4:15; Alternate Fridays.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark H. Rinehart can be reached on (703) 305-4815. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

The examiner will be relocating to a new facility on October 13, 2004. His new phone number will be (571) 272-3634 and his supervisor's new phone number will be (571) 272-3632.

JSC

MARK H. RINEHART
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100